In the Title:

Please amend the title as follows:

Mixed-Signal Core Design [[Incorporated With An SoC Having]] For Concurrent Testing of Mixed-Signal, Analog, and Digital Components

In the Specification:

Please amend the specification as follows:

Please insert the paragraph at page 1, line 1, with the following rewritten paragraph:

This application claims priority under 35 USC § 119(e)(1) of provisional application Serial No. 60/501,071, filed September 8, 2003.

Please replace the paragraph beginning at page 2, line 19, with the following rewritten paragraph:

The methodology for testing digital and analog blocks differs substantially. Digital blocks are tested for modeled defects largely using algorithmically generated test patterns, (e.g. automatic test pattern generator (ATPG) or memory built-in-self-test (memory [[M]]BIST)). On the other hand, analog blocks are tested for functionality and characterized for specific parameters. The digital test set typically comprises of scan patterns for different fault models that are applied under burn-in and voltage box [[virtual box builder]] (VBox) conditions where VBox is a condition which stresses the digital logic by changing the power supply rail voltage VDD to bring out latent defects of the digital blocks. For example, if the nominal operational voltage is 1.5V, VBox limits may be 1.1V and 2.1V. In such a case, a device may be stressed using a VDD of 2.1V volts and then tested at 1.1V to bring out a defect, which depends upon the process and the statistical data. Moreover, the digital test set includes memory tests typically in the form of memory BIST. These aforementioned digital test sets differ from I/O characterization and at-speed tests. During these tests, the device is configured into scan [[SCAN]] test mode where device functionality is lost. In contrast, during analog testing (i.e. signal-to-noise ratio (SNR) and total harmonic distortion (THD)), the tests are required to be performed only when the device is in a functional operating mode. This requirement imposes the restriction that each analog and digital block be separately and sequentially tested to avoid any conflict of the scan [[SCAN]] and functional testing.

Please replace the paragraph beginning at page 4, line 10, with the following rewritten paragraph:

The mixed-signal core includes an analog module, a first and second digital module, and a first and second virtual boundary. The analog module includes a analog components and mixed-signal components. The first digital module includes a first subset of digital components required for functional/parametric verification of the mixed-signal components within the analog module. The first virtual boundary couples between the analog module and the first digital module. The first virtual boundary having at least one multiplexer to gate signals transmitted between the analog module and the digital module. The first virtual boundary partitions the analog module from the digital module. Each multiplexer couples to receive signals generated by the analog and mixed-signal components of the analog module and the digital components of the digital module. The second digital module includes a second subset of digital components. The second virtual boundary includes at least one multiplexer to gate signals transmitted between the first and the second digital module, wherein the second virtual boundary partitions the first digital module from the second digital module. Each multiplexer of the second virtual boundary couples to receive signals generated by the first and second digital module.

Please replace the paragraph beginning at page 4, line 26, with the following rewritten paragraph:

The mixed signal core design in accordance with the present invention includes at least three modes of operation for testing the mixed signal core. The first mode of operation provides digital [[interface]] characterization testing of the first and second digital module and analog characterization/trimming testing of the analog module. To initiate this first mode of operation, the first and second virtual boundary are inactive. In a second mode of operation, concurrent testing of the analog module and the first and second digital module is conducted. Analog characterization/trimming testing is performed on the analog module and digital interface characterization testing is performed on the first digital module, while SCAN/BIST testing is performed on the second digital module. To initiate the second mode of operation, the second virtual boundary is activated to gate signals transmitted between the first and second digital module.

Please replace the paragraph beginning at page 7, line 14, with the following rewritten paragraph:

Figure 4 displays the mixed signal core 300 [[400]] designed on the SoC IC in accordance with the present invention during a functional testing mode of operation;

Please replace the paragraph beginning at page 7, line 16, with the following rewritten paragraph:

Figure 5 illustrates the mixed signal core 300 [[500]] designed on the SoC IC in accordance with the present invention during a concurrent testing mode of operation;

Please replace the paragraph beginning at page 7, line 19, with the following rewritten paragraph:

Figure 6 shows the mixed signal core 300 [[600]] designed on the SoC IC in accordance with the present invention during a non-concurrent testing mode of operation;

Please replace the paragraph beginning at page 8, line 29, with the following rewritten paragraph:

The present invention is directed to a method and structure for testing such embedded cores, particularly, analog and/or mixed-signal cores, such as an ADC and DAC in an SoC IC. Figure 3 illustrates a mixed signal core 300 designed on an SoC IC that includes a top level pin multiplexing unit 302, a mixed signal module 310 (including an analog module 312 and a first digital module 314), a second digital module 322, a data multiplexer 320, a first isolation unit 316 [[318]], a test clock generator 325 and a partition controller 330. An important criteria required for creating partitions within mixed-signal core 300 provides that the analog and mixed signal components of the mixed signal core be grouped together to form the analog module 312. In addition, a portion of the digital components, such as digital filters, that are required for the functional/parametric verification of any of the mixed-signal components, such as a sigma-delta ADC, must be grouped together to form the first digital module 314. The rest of the digital logic components and memory units within the mixed-signal core 300 are grouped together to form the second digital module 322.

Please replace the paragraph beginning at page 9, line 13, with the following rewritten paragraph:

Specifically, as shown, the top level pin multiplexing unit 302 provides characterization pin signals and external serial data to the mixed-signal module 310, data multiplexer 332 and the second digital module 322. The first isolation unit 316 couples between analog module 312 and the first digital module 314, while the second isolation unit 318 couples between the first digital module 314 and the second digital module 322. In addition, the second isolation unit 318 couples to receive a parallel test enable signal (P_T) generated by the partition controller 330. Data multiplexer 320 couples between the first digital module 314 and the second digital module 322 to provide a multiplexed data interface signal to the first digital module 314. The first digital module 314 provides a register control signal for the data multiplexer 320. The data multiplexer 320 also couples to receive the parallel test enable signal from the partition controller 330, the external serial data interface from the top level pin multiplexing unit 302, and the internal parallel data interface from the second digital module 322. Test clock generator 325 connects between the partition controller 330 and the first digital module 314 to provide a multiplexed clock. The partition controller 330 also couples to the first digital module 314 and the second digital module 322 to provide a scan [[SCAN]] signal (scan [[SCAN]]), a memory built-in self test (memory [[M]]BIST) signal (MBIST), a test clock control signal (Clk_C), a clock select signal (Select), a burn-in control signal (Burn) for analog and digital, and the parallel test enable signal (P_T), as discussed previously. The scan [[SCAN]] signal include a [[SCAN]]scan-in, [[SCAN]]scan-out, and [[SCAN]]scan-enable component. The memory [[M]]BIST signal includes a memory [[M]]BIST status and an memory [[M]]BIST control component. Within the mixed signal module 310, an analog module 312 couples to first digital module 314, wherein first digital module 314 provides a power down signal (P_D), a reset signal (Reset), a mixed-signal clock signal (Clk), an analog test signal (Test), and an analog trim signal (Trim) to analog module 312. Specifically, first isolation unit 316 couples between the analog module 312 and the first digital module to provide isolation of the data transferred between the two modules during concurrent testing using a characterization testing method upon the analog module 312 and a SCAN/BIST testing method on the first digital module 314. In operation, the parallel test enable signal generated by the partition controller 330 is used to control isolation unit 316. Test clock generator 325 receives the test clock control signal (Clk_C) an initial clocking signal from the partition controller 330. The test clock generator 325 includes a top level clock controller 324, a digital clock controller 326, and a clock multiplexer 328. The clock multiplexer 328 couples to receive the clock select signal (Select) generated by the partition controller 330.

Please replace the paragraph beginning at page 10, line 23, with the following rewritten paragraph:

The individual partitioned modules, 312, 314, and 322, are separate entities that can be configured for independent/concurrent digital and analog testing [[and tested independently and concurrently]]. This lends support to a dual (concurrent) operating mode such that normal scan and BIST tests can be applied to the digital partition unit 322, while applying functional characterization tests to the analog and digital modules, 312 and 314.

Please replace the paragraph beginning at page 11, line 11, with the following rewritten paragraph:

In a first mode of operation, the mixed-signal core 300 [[400]] of SoC IC as shown in Figure 4 includes all of the components as given in Figure 3; however, the components and connections that are activated during this first mode of operation are shaded. The first mode of operation is the normal mode of operation where functional testing is performed upon all modules 312, 314 and 322. Accordingly, functional testing is applied to the analog module 312, the first digital module 314, the second digital module 322, digital clock controller 326, and the clock multiplexer 328. These components are active as shown. The other components, the first isolation unit 318, the second isolation unit 316, the data multiplexer 332 and the top level clock controller 324, are inactive. The data signals for operating the analog module 312 and the first digital module 314 inside the mixed signal core 310 come from the CPU within the digital core (not shown).

Please replace the paragraph beginning at page 11, line 23, with the following rewritten paragraph:

In a second mode of operation, the mixed-signal core 300 [[500]] of SoC IC as shown in Figure 5 includes all of the components as given in Figure 3. Accordingly, the components and connections that are activated during this second mode of operation are shaded. Concurrent functional and SCAN/BIST testing is applied to the mixed-signal module 310 and the second digital module 322. In this second mode of operation, the [[first and]] second digital module[[s, 314 and]] 322[[, are]] is under [[SCAN]] scan test and hence its registers are programmed by scanning in the data using a serial data interface input at the chip interface as shown through top level pin multiplexing unit 302 and data multiplexer 320. The SCAN/BIST testing is selected using the [[SCAN]] scan enable component of the [[SCAN]] scan signal. Concurrently, functional tests are applied to the analog module 312 and the first digital module 314, while the SCAN/BIST tests are applied to the second digital module 322. The digital clock controller 326 provides the clocking for functional testing of the analog module 312 and first digital module 314. Isolation unit 318 provides gating of signals between the first digital module 314 and the second digital module 322. Characterization testing of the analog module 312 and the first digital module 314 is conducted by transferring of signals from the top level pin multiplexing unit 302 through the characterization pins as shown. Test clock and test control pins send test clock and test control signals to partition controller 330. Partition controller 330 generates a separate [[SCAN]]scan-in and [[SCAN]]scan-out signal along with a [[SCAN]] scan enable through the [[SCAN]] scan input of the second digital module 322. Partition controller 330 generates a separate memory [[M]]BIST signal and status control signal through the memory [[M]]BIST input to be supplied to the second digital module 322. In addition, partition controller 330 supplies a clocking signal to the top level clock controller 324. The clock multiplexer 328 provides a multiplexed clocking signal from the inputs of the top level clock controller 324 and the digital clock controller 326 to first digital module 314 which is transferred to analog module 312.

Please replace the paragraph beginning at page 12, line 19, with the following rewritten paragraph:

In the third mode of operation, the mixed-signal core [[600]] 300 of SoC IC as shown in Figure 6 includes all of the components as given in Figure 3. Accordingly, the components and connections that are activated during this third mode of operation are shaded. [[Non-concurrent functional and]] SCAN/BIST testing is applied to the first digital module 314 [[mixed-signal module 310]] and the second digital module 322. Specifically, the analog module 312 is powered down while SCAN/BIST tests are applied to the first digital module 314 and the second digital module 322. The digital clock controller 326 multiplexed with the top level clock controller 324 provides the clocking of the SCAN/BIST testing of the first digital module 314. Isolation unit 316 provides gating of signals between the first digital module 314 and the analog module 312; while isolation unit 318 provides gating of signals between the first digital module 314 and the second digital module 322. To initiate the powering down of the analog module 312, first digital module 314 provides a power down signal to analog module 312. The test clock and test control pins send test clock and test control signals to partition controller 330. The partition controller 330 generates separate [[SCAN]]scan-in and [[SCAN]]scan-out signal along with a [[SCAN]] scan enable through the [[SCAN]] scan input to be supplied to the first and second digital module, 314 and 322. The partition controller 330 generates [[separate MBIST signal and a status control signal]] memory BIST status and control signals through the memory [[M]]BIST input to be supplied to the first and second digital module, 314 and 322. In addition, the partition controller 330 supplies a clocking signal to the top level clock controller 324. The clock multiplexer 328 provides a multiplexed clocking signal to the first digital module 314. Partition controller 330 provides the burn-in control signal (Burn) along with the parallel testing control signal P_T to first digital module 314.

Please replace the paragraph beginning at page 13, line 12, with the following rewritten paragraph:

In Figure 7, the first isolation unit 316 between the analog module 312 and the first digital module 314. Isolation unit 316 provides the isolation required for signals from mixed-signal components, such as ADCs and DACs, power down signals, and clock signals. [[During, the first mode of operation where functional testing is performed, the parallel test signal PT is provided. Isolation unit 316, however, simultaneously provides some additional control.]] Specifically, isolation is required when the first digital module 314 is in the mode of operation where the SCAN/BIST [[BIST/SCAN]] testing is performed. Junk data from the ADC might enter DAC due to the SCAN/BIST [[BIST/SCAN]] testing. Similarly, the undetermined data may enter the DAC from ADC, which will affect the SCAN/BIST [[BIST/SCAN]] testing. As such, the first isolation unit 316 provides a buffer between these mixed-signal components to avoid the transfer of junk data. General purpose I/O (GPIO) pins provide a flexible parallel interface that allows a variety of custom connections and are used for this purpose. These GPIO pins are required for functional characterization testing of analog module 312.

Please replace the paragraph beginning at page 13, line 26, with the following rewritten paragraph:

Figure 8 illustrates the schematic of the second isolation unit 318 connected between the first digital module 314 and the second digital module 322. In this instance, isolation is required for the control signals, such as virtual bus (VBUS) signals. All VBUS signals (i.e. [[R]]read data, write data, clock ready, ready, byte enable, etc.) in accordance with the Change Back Acknowledgment (CBA) standard must be isolated. Thus, the external serial control interface couples to the second isolation unit 318 to provide these signals. A serial to parallel converter 318a couples to a format converter and post processing unit 318b. A multiplexer 318c couples to receive the processed serial interface signals along with the internal parallel control interface signals. The parallel test control signal P_T provides control from multiplexer 318c. This isolation is required when BIST/SCAN testing is performed the second digital module 322 and functional testing is being performed upon the first digital module 314. Since the output from second digital module 322 may contain junk data, isolation is necessary to shield the first digital module 314.

Please replace the paragraph beginning at page 14, line 16, with the following rewritten paragraph:

The proposed technique not only assists in testing under normal conditions, but also during burn-in, wherein the analog module 312 is dynamically burned using loop-back tests in the mixed-signal core 300 for additional coverage and the digital modules, 314 and 322, are burned using scan [[SCAN]] and memory BIST patterns. This is in contrast to the traditional method where the analog module 312 is powered down while the first digital module 314 is burned-in.

Amendments to the Drawings:

The attached sheet of drawings includes changes to Figures 4, 5, and 6. These sheets which include Figures 4, 5, and 6, replace the original sheets including Figures 4, 5, and 6.

Attachment: Replacement Sheets
Annotated Sheets Showing Changes